AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) An apparatus comprising:

a coreless substrate;

a layer of material attached directly to an upper side of the substrate, the layer of material having a lower elastic modulus than the substrate;

an interposer coupled to the layer of material;

a plurality of solder columns to couple the interposer to the substrate;

an integrated circuit die coupled to a plurality of solder balls; and

a capacitive layer attached to an upper side of the interposer,

wherein the interposer defines a plurality of vias to couple the plurality of solder columns to the plurality of solder balls.

2. (previously amended) An apparatus according to Claim 1, further comprising:

an integrated circuit die coupled to the capacitive layer.

3. (original) An apparatus according to Claim 2, wherein the capacitive layer is disposed between the interposer and the integrated circuit die.

4. (cancelled)

5. (currently amended) An apparatus according to Claim [4]1, the layer of material defining openings to pass the plurality of solder columns.

6. (cancelled)

7. (original) An apparatus according to Claim 1,

wherein the layer of material is laminated to the substrate.

8. (original) An apparatus according to Claim 1, further comprising:

a stiffener attached to the layer of material.

9. (original) An apparatus according to Claim 8, wherein the stiffener surrounds the interposer.

10. (previously amended) An apparatus according to Claim 1, wherein a lower side of the interposer is coupled to the layer of material.

11. (currently amended) A method comprising:

fabricating a coreless substrate;

attaching a layer of material directly to an upper side of the substrate, the layer of material having a lower elastic modulus than the substrate;

fabricating solder columns within the layer of material; ~~and~~

coupling an interposer having a capacitive layer to the layer of material~~,~~; and

fabricating a plurality of solder balls on the interposer, the interposer defining a plurality of vias to couple the plurality of solder columns to the plurality of solder balls,

wherein the capacitive layer is attached directly to an upper side of the interposer.

12. (cancelled)

13. (currently amended) A method according to Claim ~~12~~11, wherein coupling the interposer to the layer of material comprises:

coupling the interposer to the solder columns.

14. (cancelled)

15. (currently amended) A method according to Claim 11[14], further comprising:

coupling an integrated circuit die to the plurality of solder balls.

16. (currently amended) A method according to Claim 11, further comprising:

coupling an integrated circuit die to the ~~capacitive layer~~interposer.

17. (original) A method according to Claim 16, wherein coupling the integrated circuit die to the interposer comprises:

coupling the integrated circuit die to the capacitive layer.

18. (currently amended) A system comprising:

a microprocessor comprising:

a coreless substrate;

a layer of material attached directly to an upper side of the substrate, the layer of material having a lower elastic modulus than the substrate;

an interposer coupled to the layer of material;

a plurality of solder columns to couple the interposer to the substrate;

an integrated circuit die coupled to a plurality of solder balls; and

a capacitive layer attached coupled to an upper side of the interposer; and

a double data rate memory electrically coupled to the microprocessor,

wherein the interposer defines a plurality of vias to couple the plurality of solder columns to the plurality of solder balls.

19. (currently amended) A system according to Claim 18, ~~further comprising:~~wherein the ~~an~~ integrated circuit die is coupled to the capacitive layer.

20. (original) A system according to Claim 19, wherein the capacitive layer is disposed between the interposer and the integrated circuit die.

21. (cancelled)

22. (original) A system according to Claim 18, further comprising:

a stiffener attached to the layer of material.

23. (previously amended) A system according to Claim 18, wherein a lower side of the interposer is coupled to the layer of material.

24. (original) A system according to Claim 18, further comprising:

a motherboard electrically coupled to the microprocessor and to the memory.